IN THE CLAIMS:

Please amend claims 1, 10, and 13 as follows:

1. (Amended) A switch for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising:

a plurality of input ports receiving data, wherein each data comprises either TDM data or packet data;

a plurality of output ports transmitting switched data; and

a single shared memory coupling said input ports to said output ports, said single shared memory sequentially receiving all TDM data and all packet data from said input ports, said single shared memory storing both TDM data and packet data, said single shared memory switching all sequentially received TDM data and packet data from respective input ports to respective output ports, wherein switching of packet data by said single shared memory has neither latency nor jitter effect on switching of TDM data by said single shared memory, and wherein switching of TDM data is based on input time slots of said TDM data.

10. (Amended) A method for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising the steps of:

switching a TDM data from an input port to an output port, comprising the steps of:

receiving a TDM data at the input port;

determining the output port to route the TDM data;

selecting an address of a single shared memory for the TDM data based on a time slot of a frame in which the TDM data was received;

storing the TDM data at the address in said shared memory;

reading the TDM data from the address in said shared memory; and

transmitting the TDM data from the output port; and

switching a packet data from an input port to an output port, comprising the steps of:

receiving a packet data at the input port;

determining the output port to route the packet data;

selecting an address of said single shared memory for the packet data based on routing data embedded in the packet data and based on the input port which received the packet data;

storing the packet data at the address in said shared memory;

reading the packet data from the address in said shared memory; and

transmitting the packet data from the output port;

wherein switching packet data has neither latency nor jitter effect on switching TDM data.

13. (Amended) A switch for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising:

means for switching a TDM data from an input port to an output port, comprising:

means for receiving a TDM data at the input port;

means for determining the output port to route the TDM data;

means for selecting an address of a single shared memory for the TDM data based on a time slot of a frame in which the TDM data was received;

means for storing the TDM data at the address in said shared memory;

means for reading the TDM data from the address in said shared memory; and

means for transmitting the TDM data from the output port; and

means for switching a packet data from an input port to an output port, comprising:

means for receiving a packet data at the input port;

means for determining the output port to route the packet data;

means for selecting an address of said single shared memory for the packet data based on routing data embedded in the packet data and based on the input port which received the packet data;

means for storing the packet data at the address in said shared memory;

means for reading the packet data from the address in said shared memory; and

means for transmitting the packet data from the output port;

wherein switching packet data has neither latency nor jitter effect on switching TDM data.

Please add claims 15-40 as follows:

15. (New) A switch for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising;

a plurality of input ports receiving data, wherein each data comprises either TDM data or packet data;

a plurality of output ports transmitting switched data;

a shared memory coupling said input ports to said output ports, said shared memory sequentially receiving the data from said input ports, said shared memory switching a sequentially received data from a respective input port to a respective output port, wherein

switching of packet data by said shared memory has no latency or jitter effect on switching of TDM data by said shared memory;

a timeslot interchange controller coupled to said shared memory selecting addresses in said shared memory to store TDM data, said time slot interchange controller selecting an address of said shared memory for a TDM data based on a time slot of a frame in which said switch received the TDM data; and

a packet switch controller coupled to said shared memory selecting addresses in said shared memory to store packet data, said packet switch controller selecting an address of shared memory for a packet data based on routing data embedded in the packet data and based on the input port which received the packet data.

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16. (New) A switch as claimed in claim 15, wherein each data is received by an input port as a time slot in a frame.

17. (New) A switch as claimed in claim 15, wherein said shared memory comprises a TDM data memory portion and a packet data memory portion.

18. (New) A switch as claimed in claim 15, wherein said shared memory treats the input ports as logical input ports.

19. (New) A switch as claimed in claim 15, wherein said shared memory places sequentially received packet data in a queue for a respective output port.

20. (New) A switch as claimed in claim 15, wherein the data are received by said input ports and transmitted by said output ports as data exchange units.

21. (New) A switch to switch time division multiplexed (TDM) data and packet data from input ports to output ports, comprising:

a plurality of input ports to receive data, wherein each data comprises either TDM data or packet data;

a plurality of output ports to transmit switched data; and

a single shared memory coupling said input ports to said output ports, said single shared memory to receive sequentially all TDM data and all packet data received from said input ports, said single shared memory to store both TDM data and packet data, said single shared memory to switch all sequentially received TDM data and packet data received from respective input ports to respective output ports, wherein switching of any received packet data by said single shared memory has neither latency nor jitter effect on switching of any received TDM data by said single shared memory, and wherein switching of any received TDM data is based on input time slots of said TDM data.

22. (New) A switch as claimed in claim 21, wherein each data is received by an input port as a time slot in a frame.

23. (New) A switch as claimed in claim 21, wherein said shared memory comprises a TDM data memory portion and a packet data memory portion.

24. (New) A switch as claimed in claim 21, wherein said shared memory treats the input ports as logical input ports.

25. (New) A switch as claimed in claim 21, wherein said shared memory to place sequentially received packet data in a queue for a respective output port.

26. (New) A switch as claimed in claim 21, wherein the data are received by said input ports and transmitted by said output ports as data exchange units.

27. (New) A switch as claimed in claim 21, further comprising:

a time slot interchange controller coupled to said shared memory to select addresses in said shared memory to store TDM data, said time slot interchange controller to select an address of said shared memory for a TDM data based on a time slot of a frame in which said switch received the TDM data; and

a packed switch controller coupled to said shared memory to select addresses in said shared memory to store packet data, said packet switch controller to select an address of shared memory for a packet data based on routing data embedded in the packed data and based on the input which received the packet data.

28. (New) A switch as claimed in claim 21, wherein the switching of a data from a respective input port to a respective output port is controlled by a stored switch configuration.

29. (New) A switch as claimed in claim 21, further comprising:

an input data router to route sequentially data from said input ports to said shared memory; and

an output data router to route sequentially data from said shared memory to said output ports.

30. (New) A switch as claimed in claim 21, wherein the data are received by said input ports and transmitted by said output ports as data exchange units, the data exchange units for packet data comprise routing information, the switching of a data exchange unit from a respective input port to a respective output port is controlled by a stored switch configuration, said stored switch configuration uses the routing information of data exchange units for packet data to determine respective output ports to switch the data exchange units.

31. (New) A method for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising the steps of:

switching a TDM data from an input port to an output port, comprising the steps of:

receiving a TDM data at the input port;

determining the output port for the TDM data;

selecting an address of a single shared memory for the TDM data based on a time slot of a frame in which the TDM data was received;

storing the TDM data at the address in said shared memory;

reading the TDM data from the address in said shared memory; and

transmitting the TDM data from the output port; and

switching a packet data from an input port to an output port, comprising the steps of:

receiving a packet data at the input port;

determining the output port for the packet data;

selecting an address of said single shared memory for the packet data;

storing the packet data at the address in said shared memory;

reading the packet data from the address in said shared memory; and

transmitting the packet data from the output port;

wherein switching the packet data has neither latency nor jitter effect on switching the TDM data.

32. (New) The method of claim 31, wherein the preselected area of said shared memory for storing the TDM data is based on a time slot in a frame in which the TDM data was received by the input port.

33. (New) The method of claim 31, wherein the output port for the TDM data is determined based on a time slot in a frame in which the TDM data was received by the input port, and wherein the output port for the packet data is determined based on routing data embedded in the packet data and based on the input port which received the packet data.

34. (New) A switch for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising:

means for switching a TDM data from an input port to an output port, comprising:

means for receiving a TDM data at the input port;

means for determining the output port for the TDM data;

means for selecting an address of a single shared memory for the TDM data based on a time slot of a frame in which the TDM data was received;

means for storing the TDM data at the address in said shared memory;

means for reading the TDM data from the address in said shared memory; and

means for transmitting the TDM data from the output port; and

means for switching a packet data from an input port to an output port, comprising:

means for receiving a packet data at the input port;

means for determining the output port for the packet data;

means for selecting an address of said single shared memory for the packet data;

means for storing the packet data at the address in said shared memory;

means for reading the packet data from the address in said shared memory; and

means for transmitting the packet data from the output port;

wherein switching the packet data has neither latency nor jitter effect on switching the TDM data.

35. (New) A switch for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising;

a plurality of input ports to receive data, wherein each data comprises either TDM data or packet data;

a plurality of output ports to transmit switched data;

a shared memory coupling said input ports to said output ports, said shared memory to receive sequentially the data received from said input ports, said shared memory to switch a sequentially received data from a respective input port to a respective output port, wherein

switching of packet data by said shared memory has no latency or jitter effect on switching of TDM data by said shared memory;

a timeslot interchange controller coupled to said shared memory to select addresses in said shared memory to store TDM data, said time slot interchange controller to select an address of said shared memory for a TDM data based on a time slot of a frame in which said switch received the TDM data; and

a packet switch controller coupled to said shared memory to select addresses in said shared memory to store packet data, said packet switch controller to select an address of shared memory for a packet data based on routing data embedded in the packet data and based on the input port which received the packet data.

36. (New) A switch as claimed in claim 35, wherein each data is received by an input port as a time slot in a frame.

37. (New) A switch as claimed in claim 35, wherein said shared memory comprises a TDM data memory portion and a packet data memory portion.

38. (New) A switch as claimed in claim 35, wherein said shared memory treats the input ports as logical input ports.

39. (New) A switch as claimed in claim 35, wherein said shared memory places sequentially received packet data in a queue for a respective output port.

40. (New) A switch as claimed in claim 35, wherein the data are received by said input ports and transmitted by said output ports as data exchange units.